REMARKS

In the Office Action mailed December 20, 2005, the Examiner requested that the status of claims 42-45 and 49 be changed to "withdrawn" in accordance with the response to restriction requirement filed by Applicants on 10/17/2005. In response, Applicants have designated the status of withdrawn claims 42-45 and 49 to be "withdrawn."

Claims 25, 41, 46 and 48 have been objected to because of the use of the term "softPAL." Applicants have amended claims 25, 41 and 46 to include a definition of "softPAL" in a manner consistent with the Examiner's helpful suggestions. Such amendment merely makes explicit what was implicit in the claims as originally presented, and thus does not change the scope of the claims and does not relate to the prior art. Applicants have amended claim 48 to correctly refer to "dedicated elements" in place of "softPAL," thereby correcting a minor inadvertent error and rendering the present objection moot. Applicants submit that claims 41 and 46 are now in a condition for allowance, and gratefully acknowledge the allowance of the claims.

Claims 1-35 and 48 are rejected under 35 USC §103(a) as being unpatentable over Kaviani (U.S. Publication No. 2002/0079921 A1) in view of Lu et al. (U.S. Patent 6,546,539, hereafter "Lu"). Claims 36-40 and 47 are rejected under 35 USC §102(e) as being anticipated by Lu. Applicants have amended each of the independent claims to overcome the rejections. As will be described with respect to each independent claim below, Applicants respectfully submit that the claims as amended are allowable over the cited references.

Independent Claim 1

In response to the rejection of independent claim 1, Applicants have amended the claim to distinguish over the combination of Kaviani and Lu. Claim 1 relates to a method for mapping a function to logic in a programmable logic device having at least one look up table (LUT) and at least one dedicated logic element. Applicants have

amended claim 1 to indicate that the step of implementing comprises implementing the factored form of the function "according to a plurality of configurations of logic using the at least one LUT and the at least one dedicated logic element," and to include a step of "selecting a configuration of the plurality of configurations implementing the factored form of the function having the least delay." Applicants respectfully submit that Kaviani fails to disclose or suggest a method of mapping a function to logic in a programmable logic device including steps of implementing the factored form of the function according to a plurality of configurations and selecting a configuration with the least delay.

Kaviani discloses a method of optimizing the use of slices of a configurable logic block, where each slice comprises at least two function generators. After a function is factored into a sum of products, the product terms are placed in a table based upon the number of literals (i.e., inputs to a block) in descending order from the greatest number of literals to the fewest number of literals. Kaviani provides an algorithm to determine whether a given product term may be combined with another product term or a product chain in a give slice in order to reduce the number of slices. If a product term may be implemented with multiple product chains, the optimal product chain is selected by determining the product chain for which the increase in the number of inputs is minimal. (Paragraphs [0079] – [0089]). Accordingly, the goal of Kaviani is to reduce the number of slices.

However, the method of Applicants' claim 1 as amended clearly distinguishes over the combination of references by including the steps of (i) implementing the factored form of the function according to a plurality of configurations of logic using the at least one LUT and the at least one dedicated logic element, and (ii) selecting a configuration of the plurality of configurations implementing the factored form of the function having the least delay. Kaviani teaches away from implementing a function using LUTs and dedicated logic according to a plurality of configurations of logic, and selecting the configuration having the least delay, by requiring that the function be implemented in as few slices as possible (and selecting a product chain to reduce the number of inputs where a product term may be implemented in multiple product chains). That is, Kaviani teaches selecting a configuration of LUTs based upon a fixed

protocol for assigning literals of the function to the inputs of the LUTs, rather than selecting a configuration of a plurality of configurations of at least one LUT and at least one dedicated logic element having the least delay. Similarly, while Lu teaches selecting a configuration of logic which positions inputs of a factored function closer to the output of the circuit, Lu fails to disclose or suggest implementing the factored form of the function according to a plurality of configurations of logic using at least one LUT and at least one dedicated logic element, and selecting a configuration with the least delay. Accordingly, Applicants submit that independent claim 1 as amended clearly distinguishes over any combination of Kaviani and Lu. Applicants have amended claims 2 and 6 to conform the claims in view of the amendments to claim 1. Applicants respectfully request reconsideration of the rejection of claim 1 and dependent claims 2-21.

Independent Claim 22

In response to the rejection of independent claim 22, Applicants have also amended claim 22 to distinguish over the combination of Kaviani and Lu. In particular, claim 22 is directed to a programmable logic device configured to implement a function in factored form having a plurality of factored cube sets, wherein each factored cube set comprises a shared set and an unshared set. The programmable logic device of claim 22 comprises a first dedicated logic element coupling the first LUT and the second LUT to form a first LUT chain. Applicants have amended claim 22 to indicate that the first dedicated logic element couples the first LUT and the second LUT to form a first LUT chain "having a selected configuration of a plurality of configurations of the first and second LUTs and the first dedicated logic element, the selected configuration having the least delay of the plurality of configurations when configured in the programmable logic device." That is, in addition to positioning the input variables of the function having later arrival times closer to the output, the programmable logic device of claim 22 is also configured such that the LUT chain comprising the first and second LUTs and the first dedicated logic element has a selected configuration (of a plurality of configurations) having the least delay. Applicants respectfully submit that Kaviani fails to disclose or suggest a programmable logic device configured to

implement a function in factored form comprising a first dedicated logic element coupling the first LUT and the second LUT to form a first LUT chain having a selected configuration of a plurality of configurations, where the selected configuration has the least delay of the plurality of configurations when configured in the programmable logic device. Accordingly, Applicants submit that independent claim 22 as amended and dependent claim 23 are allowable over the combination of Kaviani and Lu.

Independent Claim 24

In response to the rejection of independent claim 24, Applicants have amended the claim to distinguish over the combination of Kaviani and Lu. In particular, claim 24 is also directed to a programmable logic device configured to implement a function in factored form having a plurality of factored cube sets. The programmable logic device of claim 24 as amended comprises a first dedicated logic element coupling the first combination of LUTs and the second combination of LUTs to form a first chain of combinatorial look up table (LUT) elements, wherein the first chain of combinatorial LUT elements is "selected from a plurality of configurations of chains of combinatorial LUT elements and dedicated logic elements implementing the function having the least delay of the plurality of configurations of chains." Applicants submit that the combination of references fails to disclose or suggest a programmable logic device, configured to implement a function in factored form having a plurality of factored cube sets, wherein the first chain of combinatorial LUT elements (comprising combinatorial LUT elements and dedicated logic elements) is selected from a plurality of configurations of chains of combinatorial LUT elements and dedicated logic elements implementing the function. In addition to placing input variables of the function having later arrival times closer to the output location of the function than input variables having earlier arrival times, the programmable logic device of claim 24 comprises a LUT chain selected from a plurality of configurations of chains of combinatorial LUT elements and dedicated logic elements having the least delay. Accordingly, Applicants submit that independent claim 24 as amended is allowable over the combination of references, and respectfully requests reconsideration of the rejection.

Independent Claim 25

In response to the rejection of independent claim 25, Applicants have amended the claim to indicate that a "softPAL" is a function that, when written in a sum-of-products (SOP) form, is too wide to be implemented in a single LUT but may be implemented using a combination of LUTs and dedicated logic elements, as requested by the Examiner. Applicants have also amended the claim to distinguish over the combination of references. In particular, Applicants have amended claim 25 to include a step of "determining a configuration of LUTs and dedicated logic elements, of a plurality of combinations of LUTs and dedicated logic elements, having the least delay for the at least one chain of factored cube sets." Applicants have also amended the step of implementing the at least one chain to indicate that the chain is implemented with the combination of LUTs and dedicated logic elements having the least delay. Applicants respectfully submit that the combination of references fails to disclose or suggest a method of mapping a softPAL into a programmable logic device (PLD) comprising a step of determining a configuration of LUTs and dedicated logic elements, of a plurality of combinations of LUTs and dedicated logic elements, having the least delay for the at least one chain of factored cube sets. Accordingly, Applicants submit that independent claim 25 as amended and dependent claims 26-35 are allowable over the combination of references.

Independent Claim 36

In response to the rejection of independent claim 36 as being anticipated by Lu, Applicants have amended claim 36 to clearly distinguish over Lu. In particular, Applicants have amended claim 36 to clarify that each factor of the factored form of the function is implemented by one of a plurality of lookup tables, and have further added steps of:

> "implementing the factored form of the function according to a plurality of configurations using the plurality of lookup tables and at least one dedicated logic element; and
>
> selecting a configuration of the plurality of configurations with the least delay."

Applicants respectfully submit that Lu fails to disclose or suggest either step. There is no teaching or suggestion in Lu to implement the factored form of a function according to a plurality of configurations using the plurality of lookup tables and the dedicated logic element, or selecting a configuration of the plurality of configurations with the least delay, for the same reasons set forth above with respect to claim 1. Accordingly, Applicants submit that claim 36 as amended clearly distinguishes over Lu, and that claim 36 and dependent claims 37-40 should be allowed.

Independent Claims 41 and 46

In response to the rejection of independent claims 41 and 46, Applicants have amended each claim to indicate that the softPAL is a function that, when written in a sum-of-products (SOP) form, is too wide to be implemented in a single LUT but may be implemented using a combination of LUTs and dedicated logic elements. Accordingly, Applicants submit that claims 41 and 46 as amended should be allowed.

Independent Claim 47

In response to the rejection of independent claim 47 as being anticipated by Lu, Applicants have amended claim 47 to distinguish over Lu. Claim 47 is directed to a method for decreasing delay of a node in a critical path during a mapping of a function. Applicants have amended claim 47 to include additional steps of:

> providing a cost table, in decreasing order, of estimated delays associated with a plurality of elements for mapping the function;
> implementing the function in programmable logic of a programmable logic device using a first element in the cost table; and
> implementing the function in programmable logic of a programmable logic device using the second element in the cost table.

Applicants respectfully submit that Lu fails to disclose or suggest implementing a function according to different elements of a cost table having different estimated delays, and selecting an element having a greater estimated delay if it has a smaller

delay when implemented in the programmable logic device. Accordingly, Applicants submit that claim 47 as amended clearly distinguishes over Lu and should be allowed.

Independent Claim 48

In response to the rejection of independent claim 48, Applicants have amended the claim to distinguish over the combination of Kaviani and Lu. In particular, claim 48 as amended relates to a method of mapping a function to a combination of one or more LUTs and dedicated logic elements. That is, Applicants have amended the claim to correctly refer to "dedicated logic elements" in the preamble of claim 48. Applicants have also amended the step of configuring vertical elements to recite "configuring, according to a plurality of configurations, a set of one or more vertical elements to perform a logical function." Applicants have further amended the step of mapping the FCSs to indicate that the FCSs are mapped "for each configuration of the plurality of configurations." Applicants have added a step of "selecting a configuration of the plurality of configurations having the least delay." Finally, Applicants have amended the step of coupling the one or more LUTs to comprise coupling the one or more LUTs with the one or more vertical elements according to the selected configuration. Applicants respectfully submit that the combination of Kaviani and Lu fails to disclose or suggest the steps of configuring and mapping, as amended, or the new step of selecting a configuration of the plurality of configurations having the least delay. Accordingly, Applicants submit that independent claim 48 as amended clearly distinguished over the combination of references, and should be allowed.

Conclusion

For the reasons set forth above, Applicants submit that the claims as amended are allowable over the cited art and respectfully request reconsideration.

Respectfully submitted,

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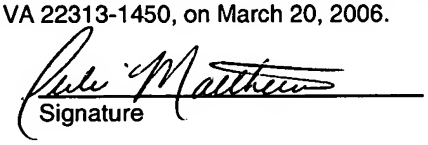

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